

WHAT IS CLAIMED IS:

1. 1. A crosspoint switch integrated circuit comprising:
 - 2 an array of input ports;
 - 3 an array of output ports;
 - 4 a switch matrix configured to selectively connect said input ports
 - 5 to said output ports for conducting electrical signals therebetween; and
 - 6 equalization circuitry coupled to at least partially offset transmission losses experienced by said electrical signal while external to said
 - 7 crosspoint switch integrated circuit.

1. 2. The crosspoint switch integrated circuit of claim 1 wherein said equalization circuitry is configured to measure jitter within said electrical signals and to utilize jitter measurements as a basis for offsetting said transmission losses, said equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization.

1. 3. The crosspoint switch integrated circuit of claim 1 wherein said equalization circuitry includes a plurality of adjustable equalizers, said adjustable equalizers each having adjustable filtering characteristics within a fixed number of equalization settings.

1. 4. The crosspoint switch integrated circuit of claim 3 wherein each said adjustable equalizer includes a plurality of switchable connections which individually adjust said filtering characteristics when activated.

1. 5. The crosspoint switch integrated circuit of claim 4 wherein each said switchable connection includes a switch, at least some of said switchable connections including at least one component which significantly affects said filtering characteristics when said switchable connections are individually activated.

1 6. The crosspoint switch integrated circuit of claim 5 wherein at least some
2 of said switchable connections are arranged in electrical parallel and said
3 components include capacitors and resistors.

1 7. The crosspoint switch integrated circuit of claim 5 wherein at least some
2 of said switchable connections are arranged in electrical parallel and said
3 components include an inductor and a resistor.

1 8. The crosspoint switch integrated circuit of claim 5 wherein said switches
2 are transistors and said components include at least some of resistors,
3 capacitors, or inductors.

1 9. The crosspoint switch integrated circuit of claim 4 wherein adjustable
2 equalizers are coupled to said input ports in one-to-one correspondence.

1 10. The crosspoint switch integrated circuit of claim 1 wherein said equaliza-
2 tion circuitry is fixed with respect to providing levels of equalization to said
3 electrical signals received at said input ports.

1 11. The crosspoint switch integrated circuit of claim 10 wherein said equaliza-
2 tion circuitry includes a dedicated circuit for each said input port, said
3 dedicated circuits being configured to provide one of a number of said levels
4 of equalization, wherein said level of equalization of a specific said dedicated
5 circuit is tailored on a basis of anticipated transmission loss for electrical
6 signals received via the input port to which said dedicated circuit is dedicated.

1 12. A crosspoint switching arrangement comprising:
2 a plurality of input ports connected to channels having non-
3 uniform frequency responses with respect to incoming signal transmissions;
4 a plurality of output ports connected to channels having non-
5 uniform frequency responses with respect to outgoing signal transmissions;
6 a switch matrix enabled to dynamically reconfigure connections
7 of said input ports to said output ports; and
8 equalization circuitry coupled to one of said input and output
9 ports, said equalization circuits having filtering characteristics that are tailored
10 on a basis of said frequency responses of said channels to which said
11 specific ones of said input and output ports are connected.

1 13. The crosspoint switching arrangement of claim 12 wherein said equaliza-
2 tion circuitry is an adaptive equalizer configured to automatically tailor said
3 filtering characteristics.

1 14. The crosspoint switching arrangement of claim 12 further comprising
2 memory configured to store equalization settings for said equalization
3 circuitry, said equalization circuitry including a separate equalization circuit
4 for each said channel for which equalization is to be applied, each said
5 equalization circuit having adjustable said filtering characteristics within a
6 fixed number of available configurations, said equalization settings stored at
7 said memory including a selection of a particular available said configuration
8 for each said equalization circuit.

1 15. The crosspoint switching arrangement of claim 14 wherein each said
2 equalization circuit includes a default configuration of first connected circuit
3 components and a plurality of alternative configurations, said default config-
4 uration achieving a first level of frequency-dependent compensation for
5 effects of skin loss in signals conducted via said channels.

1 16. The crosspoint switching arrangement of claim 15 wherein each said
2 alternative configuration introduces second connected circuit components to
3 achieve different levels of frequency-dependent compensation for said effects
4 of skin loss.

1 17. The crosspoint switching arrangement of claim 16 wherein said second
2 connected circuit components are coupled to switches that selectively
3 introduce said second connected circuit components, said switches being
4 manipulated based upon said equalization settings stored in said memory.

1 18. The crosspoint switching arrangement of claim 17 wherein said equaliza-
2 tion circuits are coupled to said input ports and are individually adjustable
3 from an exterior of an integrated circuit chip package in which said equaliza-
4 tion circuits and switch matrix reside.

1 19. A method of providing equalization for a crosspoint switch comprising:
2 determining signal characteristics related to signal transmissions
3 via each of a plurality of ports of said crosspoint switch; and
4 setting equalization circuitry housed within said crosspoint
5 switch such that each said port has filtering characteristics tailored on a basis
6 of said signal characteristics for said signal transmissions via said each port.

1 20. The method of claim 19 wherein said step of setting includes selectively
2 activating and deactivating switching devices which introduce parallel con-
3 nections of resistances and capacitances within said adjustable equalization
4 circuitry, said equalization circuitry being a plurality of adjustable equalization
5 circuits.

1 21. The method of claim 19 wherein said step of setting includes selectively
2 activating and deactivating switching devices which introduce series con-
3 nections of resistances and inductances within said adjustable equalization
4 circuits.

1 22. The method of claim 19 wherein said step of setting includes activating
2 adaptive equalization circuitry.

1 23. The method of claim 19 wherein said step of setting includes entering
2 equalization settings into an integrated circuit chip in which said equalization
3 circuitry and a switch matrix reside.

1 24. The method of claim 19 wherein said step of determining said signal
2 characteristics includes monitoring jitter at outputs of said crosspoint switch.